ABSTRACT OF THE DISCLOSURE

A semiconductor memory device comprising a redundancy circuit having a small area and high repair efficiency in which time required to store the address of a defect is short and which can reduce the manufacturing cost of the device is disclosed. Repairing addresses are sorted and stored in accordance with a specific order. In case of storing four addresses for eight addresses, a set SFG of fuses corresponding to eight decoded addresses DA0 to DA7 is provided and information indicative of the ordinal position of the fuse in the corresponding fuse-decision results which are logic 1 is used to associate the address with the repair-decision result.